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EXAMINER

KINKEAD, ARNOLD M

ART UNIT PAPER NUMBER

2817

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

10/766,730

Applicant(s)

AMMAR ET AL.

Examiner

Arnold M Kinhead

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01-28-04 Pre. Amdt.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 16-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 16-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it should be about 150 words or less. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-8, & 16-32 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 10, " the summed output" lacks antecedent basis.

In claim 16, line 6, " the frequencies" lacks proper antecedent basis. On line 7, " output frequency" should this read --output frequency signal--instead?

In claim 17, line 3, " summed output frequency" should read instead--summed output frequency signal--?

In claim 18, lines 3,4,5 and 6 same issue.

In claim 20, line 2, " the signal" lacks proper antecedent basis.

In claim 24, line 7, " the output frequencies" .

In claim 25, line 2, " said phase lock loop circuit frequency" .

In claim 27, line 4, " filtering a lower sideband" of what signal?

In claim 28, line 3, " filtering an upper sideband" of what signal?

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All other dependent claims from the above claims are indefinite too as a result.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-8 and 16-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 and 15-21 of U.S. Patent No. 6,714,089. Although the conflicting claims are not identical, they are not patentably distinct from each other because in claims 1 and 16, for example of the pending application, an apparatus and method claim are presented for a high frequency signal source, comprising a DRO, a mixer, and PLL...with means for achieving high output frequency accuracy without manual tuning; this is merely of broader scope than claims 1 and 15, respectively, in the patent (' 089). Those patented independent claims also include filtering, for example, which is covered later in application dependent claims.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1,2,3,5,6,7,8,16, 17,19,20,21,22,23,24,25,26,29,30,31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreifuss et al(US 5,940,457) in view of Ichihara(US 6,587,005) and further in view of Wong(US 5,768,693).

The reference by Dreifuss et al discloses a high frequency signal source(synthesizer) see figure 3, which comprises a DRO(dielectric resonator,38) with output signal that is sent to a mixer(34). A PLL circuit with VCO(42) is shown connected to said mixer and the mixer outputs the (sum and difference components)summed output frequency which is coupled into the phase lock loop to allow for quicker stabilization to new frequencies when frequency shifting is required. A crystal reference oscillator is shown(18)(claims 2,29).

Dividers (16,30) are shown in the PLL circuit with one dividing by a factor(N), as noted in col. 8, lines 16-22, these maybe programmable dividers(cls. 6,7,8,21,22,23,30 and 31 in part).Ucontoller (26,28) is shown for controlling the dividers(16,30). An amplifier(32) is shown connected to the mixer(34)(cls. 5,20).. The method steps being inherent to the structure.

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The reference does not show a free running DRO, i.e. a DRO without PLL as shown in the above reference(38), as well as being stabilized(in view of temperature changes, etc.) despite being a free run oscillator; no filter is shown on the mixer output(cls.3,17 19). Also not highlighted is the use of registers with controller for providing the programmable divider(s) on a PLL chip. With regards the latter, that is implementing the dividers with registers that may be programmable, the reference by ^{Tchihara} Ichihara, see figure 6 and col. 7, lines 1-30, exemplifies the integrated PLL with registers, i.e., each of the major chip elements in the loop, registers(18,19) for controlling dividers, and controller(20) are part of the LSI chip. The PLL circuit has been integrated to include one or more of the loop elements on chips to achieve a more compact and flexible package.

With regards the free run type DRO The reference by Wong, from the same field of endeavor, does show DRO oscillators(30-33,see col. 4, lines39-42) in a bank(29), see figure 2, that are free running, in that they are not in a PLL feedback loop. As noted in col. 5, lines 53-65, the oscillators may be controlled, in light of temperature change and ageing, by way of controlling an amplified mixer output of a PLL. The oscillators are not part of the PLL and therefor are free running. Note amplifier on the output. This output will be coupled to the mixer of the PLL in Dreifuss et al. Please note filter on mixer(41) output for bandpass filtering as is conventional for selecting desired frequencies.

In light of the above it would have been obvious for one of ordinary skill in the art to have modified the reference by Dreifuss et al showing a PLL-DRO synthesizer, to make use of conventional programmable dividers on a PLL chip so as to allow for frequency control and a more compact package overall with various elements being integrated in a chip package, as exemplified by Ichihara. The use of programmable registers being notoriously well known in the art as noted above for providing the divider operation. Also, using a free running DRO with compensation for temperature and ageing is shown by Wong and could serve to replace the PLL-DRO((38) of

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Dreifuss et al, both being used in FSK systems and achieve the same high frequency stabilized output with the ability to change frequencies rapidly with less complexity.

Allowable Subject Matter

4. Claims 4 , 18, 27,28 and 32 would be allowable if rewritten to overcome the rejection(s) under 35

U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. High side and low side filtering not suggested in the prior art in addition to all else claimed. Upper sideband filtering(cl.28) not suggested. And for claim 32, no fair suggestion for the biasing of a transistor...

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Arnold M Kinkead

Primary Examiner

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Arnold Kinkead

Oct. 06, 2004